The Future of PCB Design

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Ten years ago, advanced PCB design technologies such as microvias, high-density interconnect (HDI), embedded passives and high pin-count field programmable gate arrays (FPGAs) were mainly available to power users designing bleeding-edge products for global organizations. Not only are these design technologies rapidly making their way into the mainstream design world, they are readily available, affordable and are a primary factor in determining a company's success and profitability.

While the availability of these design technologies is growing at an accelerated rate (see Figure 1), they are concurrently introducing increased design complexity and design challenges. Particularly in the high-speed design arena, data rates of 3 gigabits/second and higher (up to 10 gigabits/second) are re-setting frequency standards for integrated circuits (ICs) including FPGAs.
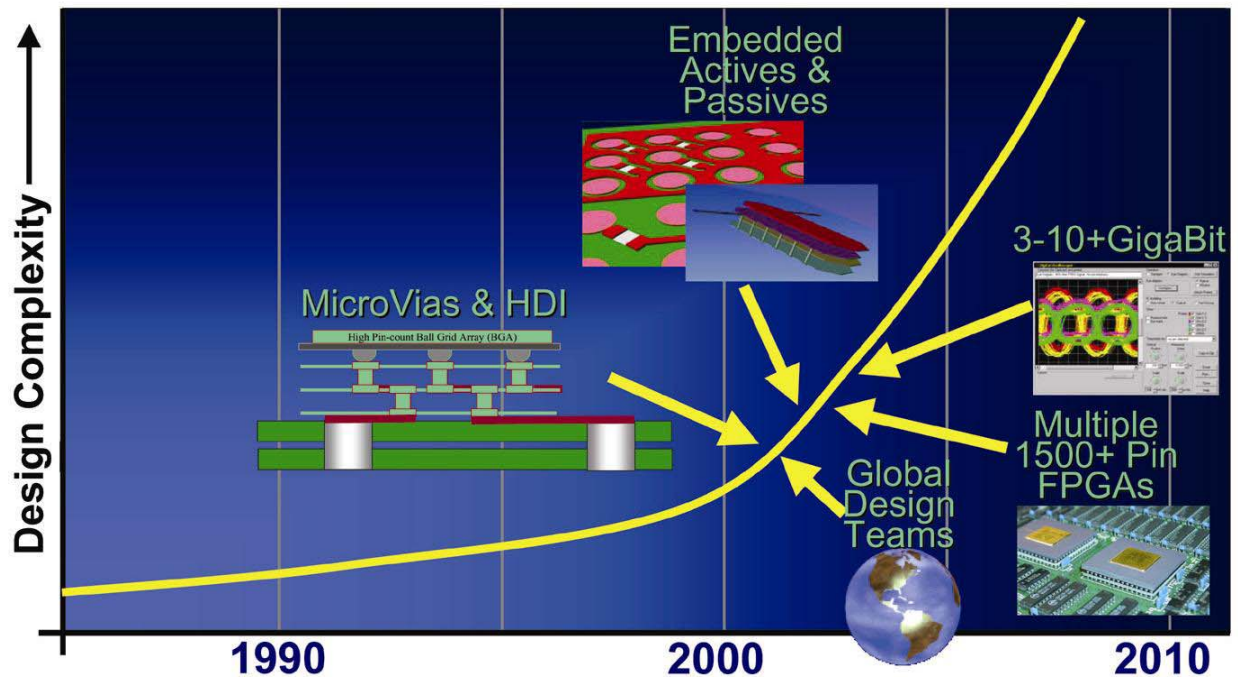

Figure 1: PCB design complexity is increasing at an accelerated rate.

As such, most of today's PCBs are pushing, if not exceeding, the limits of classic board design. In mobile telecom, for example, interconnect and board dimensions are shrinking rapidly, while designs are utilizing fewer, but more complex (and higher pin-count) components. At the same time, boards for networking and computer applications are getting larger, with more interconnect and plane layers.

In order to produce higher quality, more-complex products, quicker and more cost-effectively than their competition, companies are taking inventory of their PCB design tools. Understanding which tools best support the needs of design teams is key to determining the proper infrastructure investment, required services, support structure and intellectual skill set of the company.

Advanced functionality already exists in today's leading design tools to solve current and future design challenges. Therefore, companies effectively utilizing the proper design tools (or combination of tools) have an advantage over those companies using dated technology to design their boards—the inherent ability to automatically solve design challenges without workarounds or short-term, inefficient solutions.

This paper discusses current and future trends in high-speed design; PCB fabrication, design and interconnect; FPGA-on-board integration; team design; and library, constraint and data management—addressing challenges and solutions associated with each area and the underlying PCB design industry.

High-Speed Design

As previously mentioned, data rates of 3 gigabits/second and higher (up to 10 gigabits/second) are re-setting performance standards for ICs. As IC and FPGA vendors replace parallel bus architectures with serial asynchronous architectures, traditional high-speed design challenges such as delay, timing, crosstalk and overshoot are replaced by challenges such as jitter, lossy lines and bit error rates. In other words, for today's high-speed routing and verification processes, following "rules of thumb" is no longer a reliable (or viable) design practice.

Standards for encoding and decoding electrical signals in serial asynchronous architectures are utilized by the relatively new 3rd-Generation Input-Output (3GIO) technology (see Figure 2). Already, Intel Corporation has incorporated 3GIO technology into its PCI Express™ standardization environment. A recent industry-wide survey (see Figure 2a) shows that 14 percent of today's PCBs are currently operating in the 1-10GHz frequency range where this architecture is prevalent.
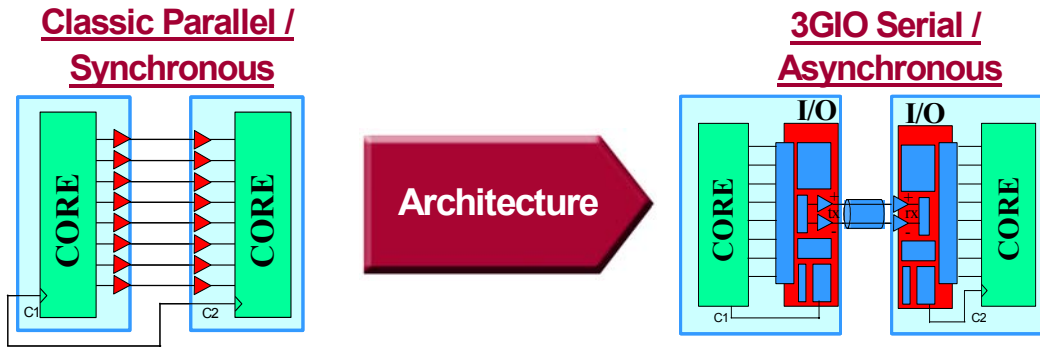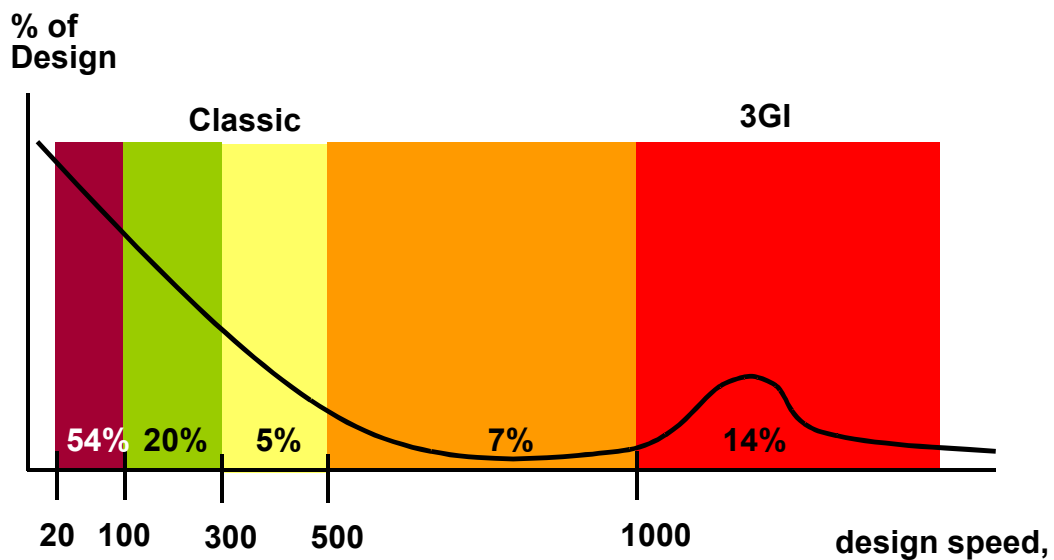
Figure 2: Inter-IC and FPGA communication is adopting new architectures to achieve speeds greater than 500MHz.

Source: EE Times 2003 EDA Study

Figure 2a: Higher-frequency, high-speed designs are growing in number.

From a PCB design perspective, the majority of today's high-speed design tools lack the advanced modeling and verification requirements utilized by 3GIO technology. With the onset of serial asynchronous architectures, these tools must further accommodate new design concepts for routing highly constrained differential pairs.

High-speed design tools from Mentor Graphics currently utilize sophisticated constraint management, multi-lingual device modeling, advanced signal integrity (SI) verification, symbolic timing analysis, rules-driven tuning and analysis-driven routing that both meet advanced IO architecture standardization requirements and address design challenges associated with 3GIO technology.

PCB Fabrication, Packaging and Interconnect

Until recently, most design teams used traditional laminate structures and vias (both through and blind vias) during PCB fabrication, packaging and interconnect. However, today's high-density, high pin-count IC packages (such as ball grid arrays (BGAs), chip on board (COB) and chip scale packages (CSPs)) are driving the need for build-up structures and microvia technology (see Figure 3).
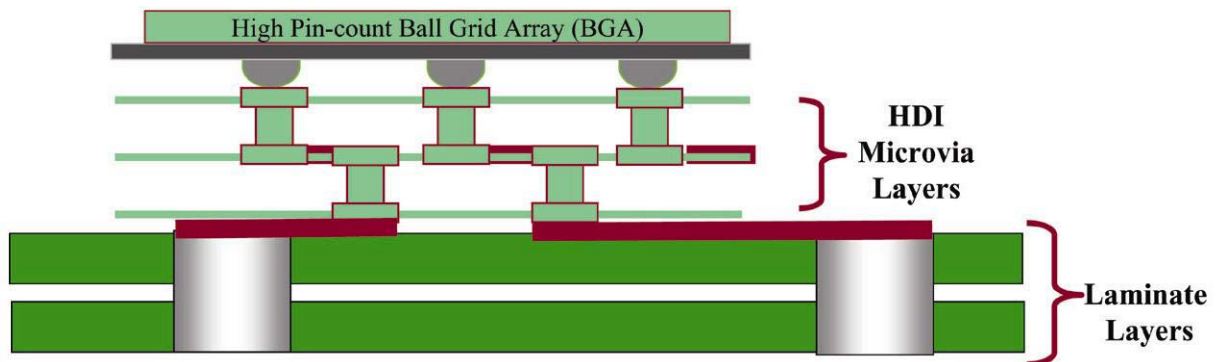

Figure 3: High-density, high pin-count IC packages are driving the need for high density interconnect (HDI) layers.

A major benefit to using high-density, high pin-count IC packages with build-up material and microvia technology is the ability for companies to produce smaller PCBs. And with the advances in build-up material and microvia technology, companies are also incorporating embedded passives (resistors, capacitors and inductors that are embedded within laminate layers, as opposed to mounted on either surface of the PCB) into their designs. To a great degree, this trend is driven by increasing passive component requirements for ICs (see Figure 4) and FPGAs, which is also driving down the price of embedded components across the industry.
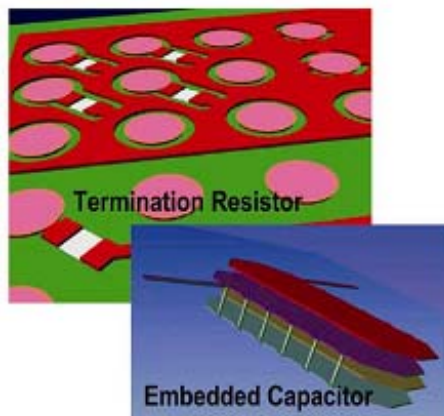

Figure 4: Increasing requirements for embedded passives in PCBs.

As with build-up material and microvia technology, incorporating embedded passives into a design opens more space on the surface layers of a PCB (concurrently reducing the overall size of the board)—resulting in additional cost savings on laminate material.

To successfully reap the benefits associated with build-up material, microvias and embedded passives, PCB design tools must utilize true 45-degree routing, localized rule definition, complex rules for microvia routing, advanced interconnect and the automation of large device geometry/footprint creation. This includes accounting for fine-pitch parts, mixed routing rules, specialized algorithms and place and route inside the laminate material.

FPGA-on-Board Integration

As the up front manufacturing costs of application specific integrated circuits (ASICs) continue to increase, and as the cost, density and performance of FPGAs improves, PCB design teams are integrating more FPGAs into their board designs. In fact, it is no longer uncommon to find boards containing one or more FPGAs with over 1500 pins.

The design of PCBs and FPGAs continues to occur concurrently, yet independently, achieving tight integration between the two designs is critical to shortening a product's overall time-to-market. Strategic alliances between PCB design tool vendors and FPGA vendors are facilitating communication between the two design processes, and ultimately paving the way for advanced FPGA device modeling (for signal integrity and timing) and high pin-count symbol and part creation.

The following PCB/FPGA integration is possible today: (1) creation and fracturing of PCB schematic symbols and geometries directly from the FPGA design tool and (2) management of design constraints and pin-out assignments between the PCB and the FPGA (for any number of FPGAs) (see Figure 5). This integration not only automates manual (and tedious) design processes, it reduces routing and timing problems once associated with traditional FPGA-on-board integration.
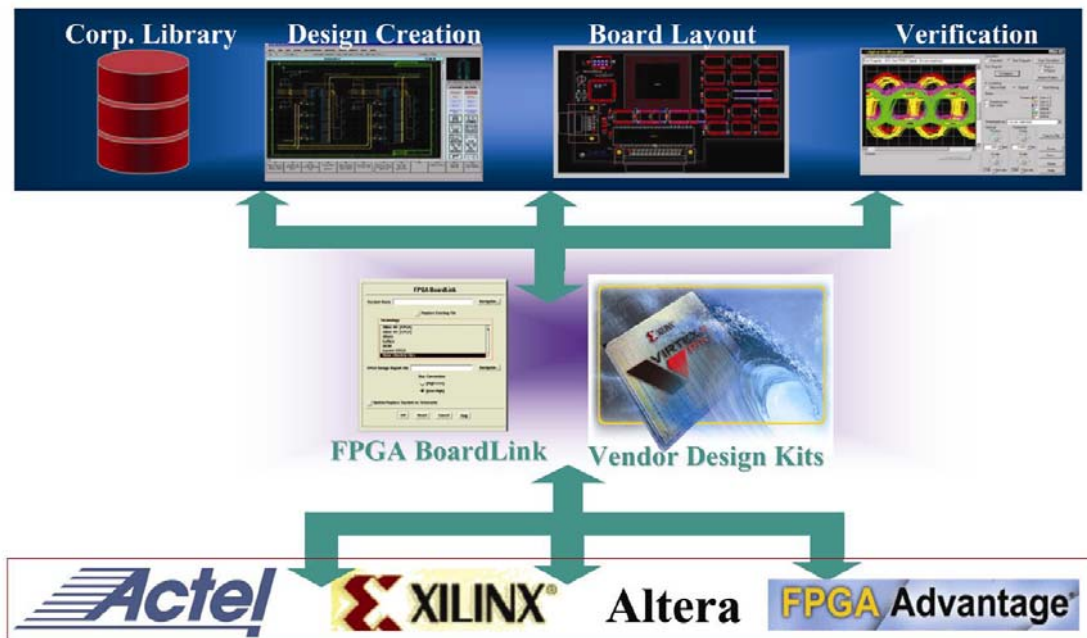
Figure 5: Tight integration between PCB and FPGA design processes.

Strategic alliances between PCB design tool vendors and FPGA vendors are also being credited for the influx of FPGA design kits that are driving PCB layout and high-speed verification and analysis. FPGA design kits typically include buffer models, component footprints, constraint rules and reference designs.

For example, the RocketIO™ design kit from Xilinx, Inc. and Mentor Graphics includes all of the qualified example circuits, connector and transmission line trace models required to simulate multi-gigabit transceivers (MGTs) when incorporating Virtex-II Pro™ FPGAs into a PCB design. By eliminating the need for SPICE expertise, the design kit allows Mentor Graphics ICX™ and HyperLynx® GHz design tool users to easily perform SI analysis on boards using a wide range of interconnects, from traditional parallel interconnects, to state-of-the-art multi-gigabit serial interconnects.

Team Design

In industries where time-to-market is a critical driver (that is, most industries), companies are utilizing concurrent / parallel design techniques during multiple stages of the PCB design process.

One traditional approach to concurrent design is to establish an around-the-clock or around-the-world design schedule. In reality, however, these approaches are more serial than parallel, as increasing design complexities require the constant presence of the design engineer during the layout process. Therefore, the schedule breaks down if the design engineer is not available (asleep, in a different time zone, or both).

6

New team design methodologies allow multiple designers to work simultaneously on the same design layout (see Figure 6). In a nutshell, reserved areas are drawn on a board, which is then split into partitions that are assigned to various team members. During the design process, team members can view and respond to the work their peers are contributing towards their respective partitioned areas and the overall master design.
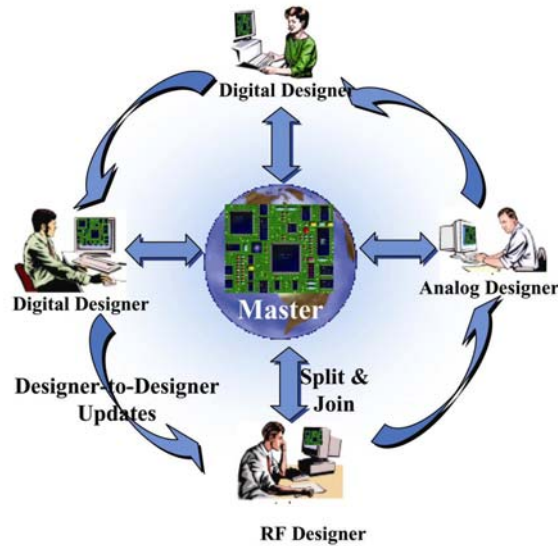

Figure 6: Team design methodologies enable concurrent / parallel, PCB design.

The measurable benefits of this new team design methodology are numerous and wide-ranging. Not only is design cycle time greatly reduced through parallel design processes; it facilitates design team collaboration, effective resource management, layout design time reduction and functional design specialization (where functional design specialists are able to simultaneously design mixed-technology boards—combining analog, digital and RF design data, for example).
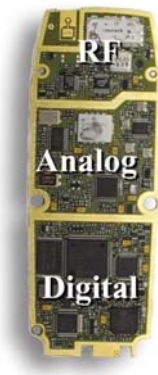

Figure 7: Many PCBs contain a mixture of RF, digital, and analog.

The team design methodology also eliminates quality and design time issues associated with manual workarounds (that is, ASCII database manipulations). For designs that are too large or complex to complete in a desired time frame, team design enables collaboration across geographically dispersed and/or functionally organized PCB design groups, further maximizing productivity and dramatically shortening time-to-market.

Library, Constraint and Data Management

Electronics companies typically make large investments in PCB design tools, libraries, infrastructure, design data and designers. These companies may have sites worldwide, and even design teams working on the same projects at several locations. Therefore, cost reduction is key to remaining competitive in a global business environment. From a PCB design perspective, high return on investments is associated with effective library, constraint and design data management.

For example, many companies utilize several different design tools throughout their design process. PCB design tools typically adhere to numerous rules (constraints) for layout, high-speed design, manufacturing and test (to name a few). These tools tend to require the same constraint information in different formats. This information is usually entered manually into each of the various design tools—a potentially time-consuming and error-prone process.

Not to mention, the onset of high pin-count devices mandates additional (complex) constraint information be entered into design libraries. Consequently, design librarians are stretching themselves thin, and the management of work-in-process (WIP) design data and release management is suffering.

In response to these challenges, many companies are implementing constraint management systems to manage constraint data integration throughout the design process (see Figure 8). Additionally, design data management systems are being used to manage both proprietary business information and overall design infrastructure.
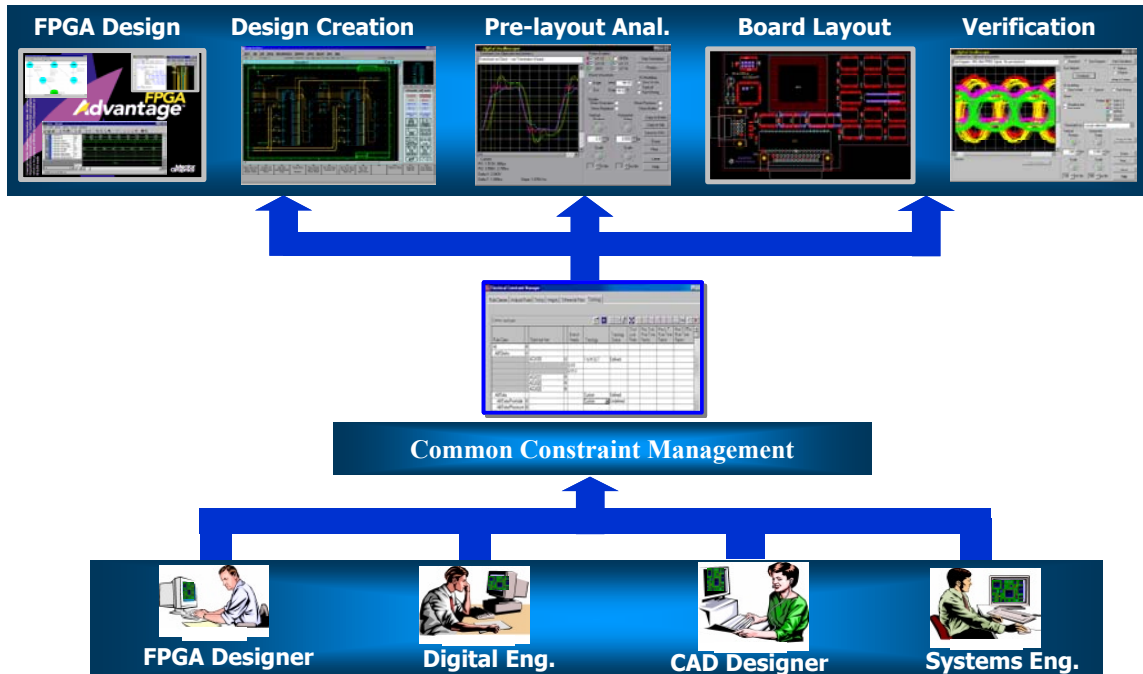
Figure 8: Constraint management systems manage data integration throughout the design process.

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Understanding current and future PCB design challenges in all areas of PCB design (from high-speed design; PCB fabrication, design and interconnect; FPGA-on-board integration; team design; to library, constraint and data management) is a critical aspect of a company's investment in a PCB design solution. PCB design tools currently containing advanced functionality to meet these challenges provide companies with an automatic advantage over those companies using dated technology to design their boards—the inherent ability to automatically solve design challenges without workarounds or short-term, inefficient solutions. Understanding which PCB design tools best support the needs of design teams is key to determining the proper infrastructure investment, required services, support structure and intellectual skill set of the company. In the end, these companies tend to produce higher quality and more-complex products, quicker and more cost-effectively than their competition.

For more information and white papers visit the following URLs:
- FPGA-on-board: http://www.mentor.com/fpga_boardlink/.
- Design and data management: (http://www.mentor.com/dms)
- Team design: (http://www.mentor.com/teampcb)
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