FPGA
How do they work?

ETI135, Advanced Digital IC Design

Anders Skoog, Stefan Granlund 21-02-2012

Content

- What is a FPGA?
- How FPGAs work
- Manufacturers
- Distributed RAM
- History
- FPGA vs ASIC
- FPGA and Microprocessors
- Alternatives to FPGAs

What is a FPGA?

- Field-Programmable Gate Array
- Digital logic chips that can be reconfigured so that they preform a logic function
- Programmed with HDL languages e.g. VHDL or Verilog

[B1]

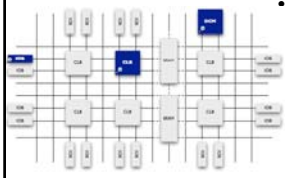
FPGA

Typical applications

- Aerospace & Defense
- Automotive
- Medical/Scientific
- Storage & servers
- Wired & wireless communications

How FPGAs work

FPGA Design

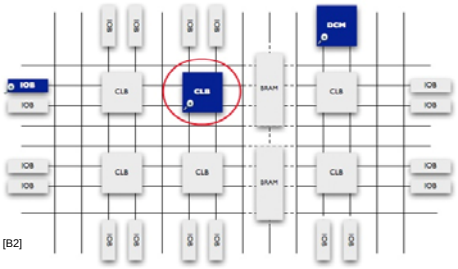


[B2]

- Block structure
  CLB (Configureable Logic Block)
  RAM
  IOB
  DSP
  Microprocessors
  Multipliers

How FPGAs work

Cont



[B2]

How FPGAs work

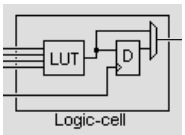
Cont

Logic-Cell

Smallest part in FPGA

Consists at least of
- Lookup Table (4-6 inputs)
- D-flipflop
- MUX

[B3]

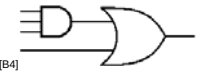


How FPGAs work

Cont

Behaviour to duplicate

3-input AND & OR



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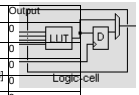
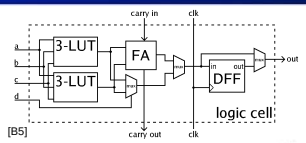
Lookup on FPGA

Input	Output
0000	0
0001	0
0010	0
0011	0
0100	0
0101	0
0110	0
0111	1
1000	1
1001	1
1010	1
1011	1
1100	1
1101	1
1110	1
1111	1

[B3]



How FPGAs work
Cont



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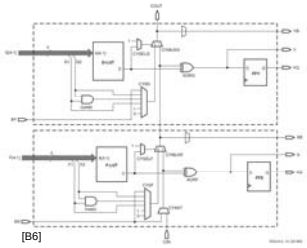
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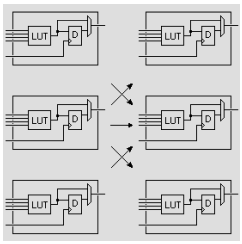
How FPGAs work
Cont

Several Logic cells then gets interconnected



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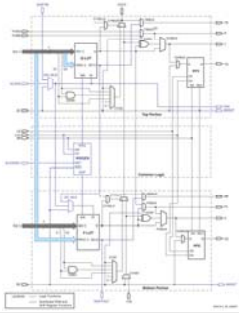
How FPGAs work
Cont

Logic Cells can be connected to slices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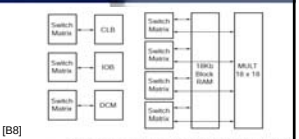
Several Slices form a CLB

How FPGAs work
Cont

Interconnections between blocks is managed with Switch Matrices



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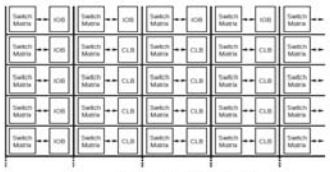
Four Types of Interconnect Tiles (CLBs, IOBs, DCMs, and Block RAM/Multiplier)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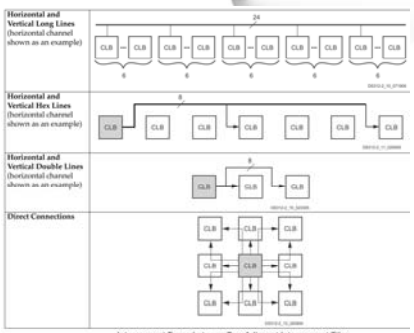
Array of Interconnect Tiles in an FPGA

How FPGAs work
Cont

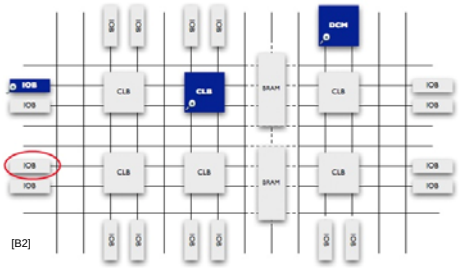
Interconnections between two adjacent CLB



Interconnect Types between Two Adjacent Interconnect Tiles

[B17]

How FPGAs work
Cont



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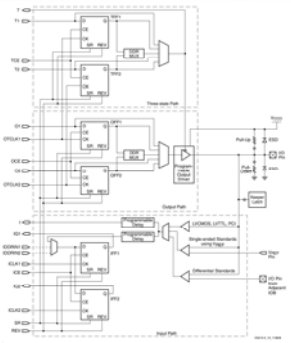
How FPGAs work
Cont

IOB



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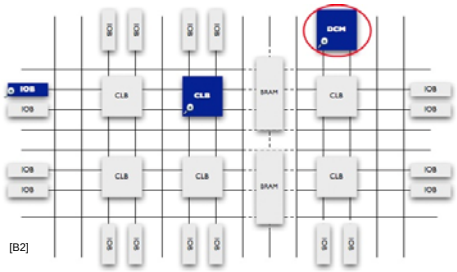
How FPGAs work
Cont



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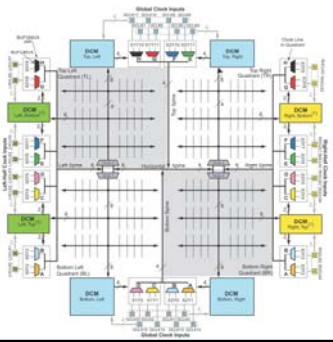
How FPGAs work
Cont



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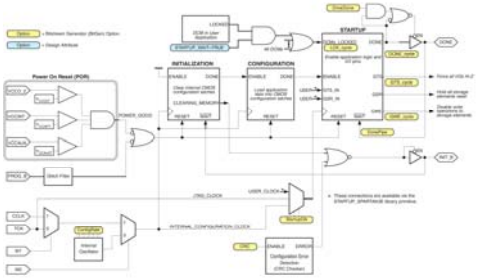
How FPGAs work
Cont

Configuration of FPGA

- The FPGA clears (initializes) the internal configuration memory
- Configuration data is loaded into the internal memory
- The user-application is activated by a start-up process

How FPGAs work
Cont

Configuration of FPGA



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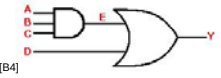
How FPGAs work
Cont

Example of VHDL-code



[B4]

```
LIBRARY ieee;
USE ieee,std_logic_1164.all;
use IEEE.NUMERIC_STD.all;

ENTITY LogicUnit IS
    PORT(
        A           : IN    STD_LOGIC;
        B           : IN    STD_LOGIC;
        C           : IN    STD_LOGIC;
        D           : IN    STD_LOGIC;
        Y           : OUT   STD_LOGIC);
    );
END LogicUnit;

ARCHITECTURE behav OF LogicUnit IS

signal E        : STD_LOGIC;

begin

process(A,B,C)
begin
    E = '0';
    if (A = '1' AND B = '1' AND C = '1') then
        E = '1';
    end if;
end process;

process(D,E)
begin
    Y = '0';
    if ( D = '1' OR E = '1') then
        Y = '1';
    end if;
end process;

END ARCHITECTURE behav;
```

Design Flow

1. Describe function in HDL or Schematic
2. Simulate
3. Synthesize and create netlist
4. Simulate with netlist
5. Place and Route
6. Simulate/verify Place and Route
7. Generate binary files
8. Upload to FPGA via JTAG interface or to a external memory device

IP-Cores

- IP-Cores are a reusable unit of logic, cell, or chip layout design that is the intellectual property of one party.
- Soft cores: HDL code or as an Netlist
- Hard cores: ASICs embedded on FPGA
- FFT, AC97, ARM processors, MIPS, MP3 codec
- Opencores.org

Manufacturers

Major manufacturers (80% of market):
- Xilinx (over 50% of market)
- Altera

Other manufacurers:
- Lattice semiconductor
- Actel
- SiliconBlue
- QuickLogic

ref. [1]

Xilinx vs Altera

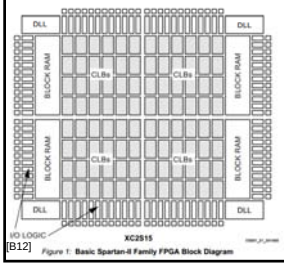
Design philosophy

Xilinx:
Tries to include as many features as possible, at the cost of increasing the complexity of the FPGA.

Altera:
Include the features most people use, to keep the complexity down.

Xilinx vs Altera
RAM-implementation

- Xilinx and Altera use "big" RAM-blocks
- Xilinx uses "Distributed RAM" for small RAMs
- Altera mixes smaller and bigger blocks of RAM



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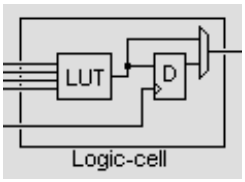
[B16]

Distributed RAM

- Xilinx patented technology
- Turns a Logic-cell in to a small 16bit RAM, ROM or FIFO shift register

[B3]



History
FPGA patent

- Invented by Ross Freeman
- Patent filed in in 1984 describing basic FPGA functions

"Patent No. 4,870,302 -- Each configurable logic element in the array is in itself capable of performing any one of a plurality of logic functions depending upon the control information placed in the configurable logic element. Each configurable logic element can have its function varied even after it is installed in a system by changing the control information placed in that element. "

Ref. [2]

History
First commercially viable FPGA

- XC2064
- 1985
- By co-founders of Xilinx Ross Freeman and Bernard Vonderschmitt
- 64 CLB with two 3-input lookup tables
- Today: Virtex 7 ~150 000 CLB with four 6-input lookup tables

Ref. [2] [3]

FPGA vs ASIC
FPGA advantages

- Simpler design cycle
- No "non recurring expenses"
- More predictable project cycle
- Reprogrammable
- Shorter time to market, 9 months compared to 2 years

Ref. [5]

FPGA vs ASIC
ASIC advantages

- Dynamic power: ASIC 12 x less than FPGA
- Area: ASIC 40 x less than FPGA
- Speed: ASIC 3.2 x faster than FPGA
- Full custom capabillity
- Lower unit cost

Ref. [4]

FPGA vs ASIC
What to choose?

ASIC
- High volume products
- Low power products
- High speed

FPGA
- Low to medium volume products
- Needs to be flexible
- Short development time

FPGAs and Microprocessors

- Combining Serial and parallel processing
- Reconfiguring FPGA at "run-time"
- Loading firmware at Power on

[B13]

FPGAs and Microprocessors

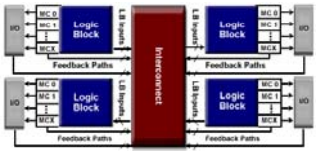
Hardware processor embedded in FPGA
- PowerPC
- ARM Cortex-M3
- Atmel

Soft processor core
- MicroBlaze
- Nios II

CPLD

Alternative to FPGA

- Macocells with logic-gates and flip-flops
- Non-volatile configuration memory
- Constant signal delay
- Not as flexible as FPGAs
- Less number of gates than a FPGA



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Thank you for listening

Questions?

References

Text

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References

Pictures

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